

General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It combines one N channel MOSFET and one P channel MOSFET

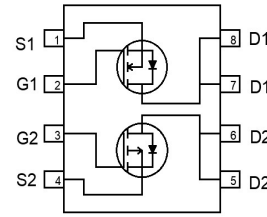
Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Dual DIE in one package
- Low Thermal resistance

Application

- BLDC Motor driver
- Load switch

Product Summary



$$V_{DS1} = 20V$$

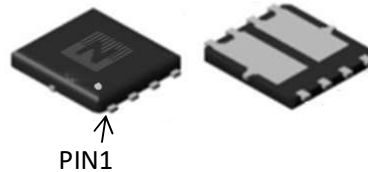
$$V_{DS2} = -20V$$

$$R_{DS(ON)1} = 35m\Omega$$

$$R_{DS(ON)2} = 65m\Omega$$

$$I_{D1} = 5.5A$$

$$I_{D2} = -4A$$



DFN3*3



Ordering Information:

Part NO.	ZMCA88201M
Marking	C88201
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

N Channel Absolute Maximum Ratings ($T_C=25^{\circ}C$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		20	V
Gate-Source Voltage ^①	V_{GS}		± 12	V
Continuous Drain Current	I_D	$T_C=25^{\circ}C$	5.5	A
	I_D	$T_C=75^{\circ}C$	5.5	A
	I_D	$T_C=100^{\circ}C$	5.5	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^{\circ}C$;	16.5	A
Total Power Dissipation	P_D	$T_C=25^{\circ}C$	17	W
Total Power Dissipation	P_D	$T_A=25^{\circ}C$	2.5	W
Operating Junction Temperature	T_J		-55 to +175	$^{\circ}C$
Storage Temperature	T_{STG}		-55 to +175	$^{\circ}C$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1mH$, $V_{GS}=4.5V$, $R_g=25\Omega$,	10	mJ
ESD Level (HBM)			CLASS 1B	

•P Channel Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		-20	V
Gate-Source Voltage ^②	V_{GS}		± 12	V
Continuous Drain Current	I_D	$T_C=25^{\circ}\text{C}$	-4	A
	I_D	$T_C=75^{\circ}\text{C}$	-4	A
	I_D	$T_C=100^{\circ}\text{C}$	-4	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^{\circ}\text{C}$;	-12	A
Total Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$	17	W
Total Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	2.5	W
Operating Junction Temperature	T_J		-55 to +175	$^{\circ}\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^{\circ}\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=-4.5\text{V}$, $R_g=25\Omega$,	10	mJ
ESD Level (HBM)	CLASS 1B			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	8.6	$^{\circ}\text{C/W}$
Thermal resistance, junction-ambient ^③	R_{thJA}		-	60	$^{\circ}\text{C/W}$
Soldering temperature	T_{sold}		-	260	$^{\circ}\text{C}$

•N Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	0.5	0.7	1.2	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=20V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=2A$		35	55	m Ω
		$V_{GS}=4.5V, I_D=1A$		40	65	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=1A$		10		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=2A$			1.3	V

•N Channel Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=10V$	-	471	-	pF
Output capacitance	C_{oss}		-	58	-	
Reverse transfer capacitance	C_{rss}		-	45	-	
Gate Resistance	R_g	$f=1MHz$	-	1.8		Ω
Total gate charge	Q_g	$V_{DD}=10V, I_D=1A, V_{GS}=4.5V$	-	4.8	-	nC
Gate - Source charge	Q_{gs}		-	1.4	-	
Gate - Drain charge	Q_{gd}		-	2.3	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DS}=10V, R_G=3.3\Omega, I_D=1A$	-	9	-	ns
Turn-ON Rise time	t_r		-	4.2	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	13	-	ns
Turn-Off Fall time	t_f		-	2.6	-	ns

•P Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.5	-0.7	-1.2	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-20V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-2A$		65	100	m Ω
		$V_{GS}=-4.5V, I_D=-1A$		85	120	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_{SD}=-1A$		8		s
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=-2A$			1.3	V

•P Channel Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=-10V$	-	495	-	pF
Output capacitance	C_{oss}		-	64	-	
Reverse transfer capacitance	C_{rss}		-	51	-	
Gate Resistance	R_g	$f=1MHz$	-	8		Ω
Total gate charge	Q_g	$V_{DD}=-10V,$ $I_D=-1A,$ $V_{GS}=-4.5V$	-	5.3	-	nC
Gate - Source charge	Q_{gs}		-	1.5	-	
Gate - Drain charge	Q_{gd}		-	2.4	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=-4.5V, V_{DS}=-10V,$ $R_G=3.3\Omega, I_D=-1A$	-	11	-	ns
Turn-ON Rise time	t_r		-	5.6	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	15	-	ns
Turn-Off Fall time	t_f		-	5.7	-	ns

• N Channel characteristics curve

Fig.1 Gate-Charge Characteristics

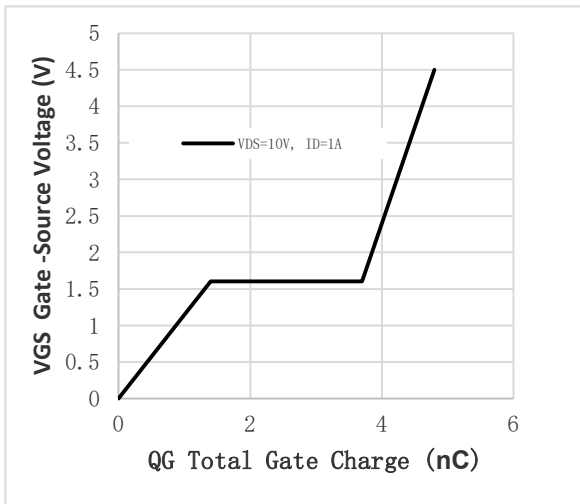


Fig.2 Capacitance Characteristics

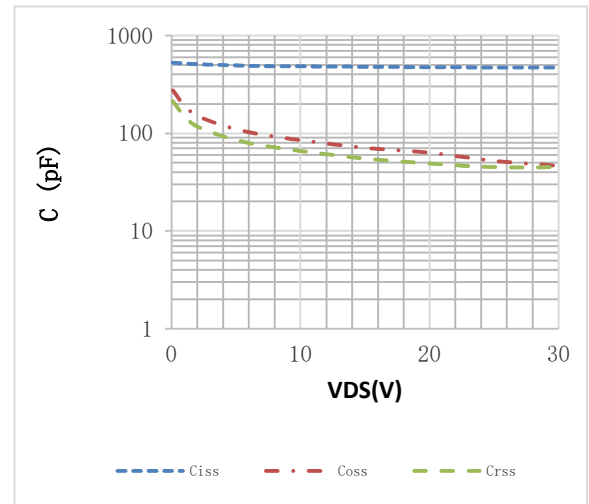


Fig.3 Power Dissipation

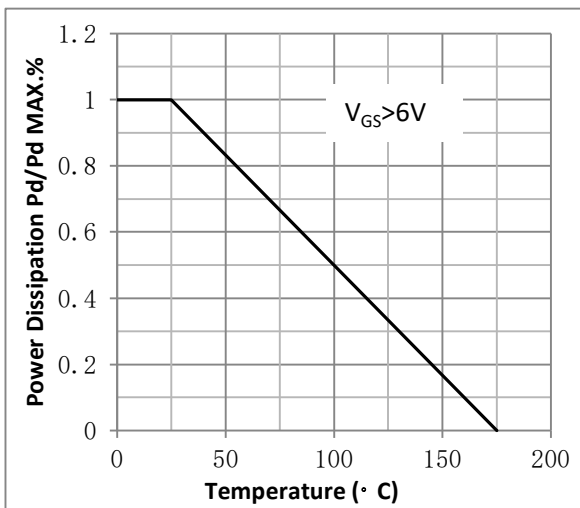


Fig.4 Typical output Characteristics

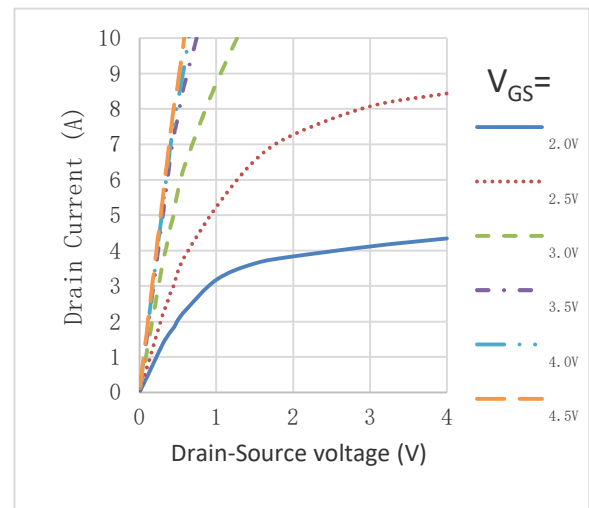


Fig.5 Threshold Voltage V.S Junction Temperature

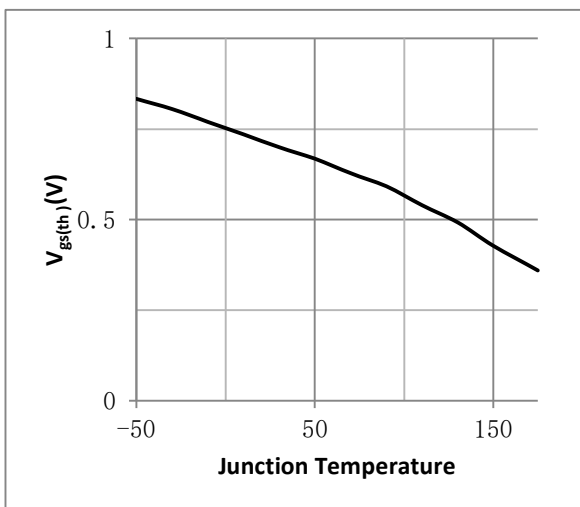


Fig.6 Resistance V.S Drain Current

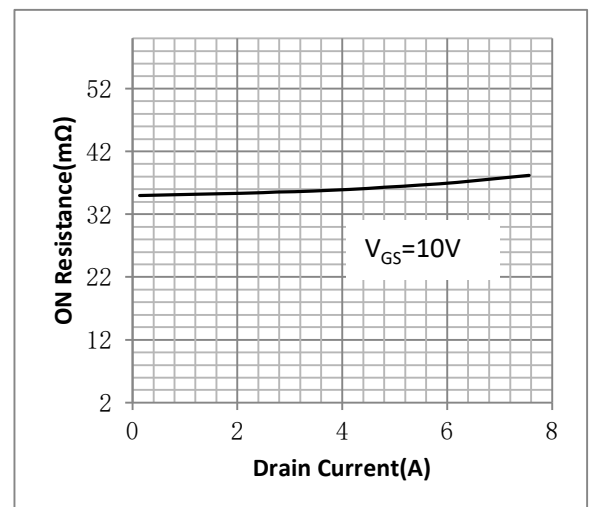


Fig.7 On-Resistance VS Gate Source Voltage

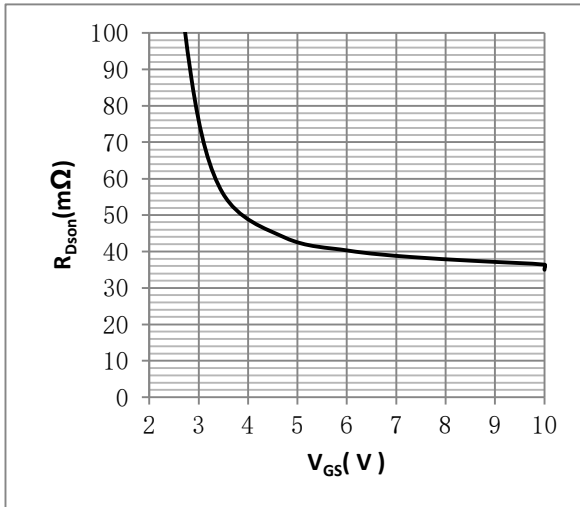


Fig.8 On-Resistance V.S Junction Temperature

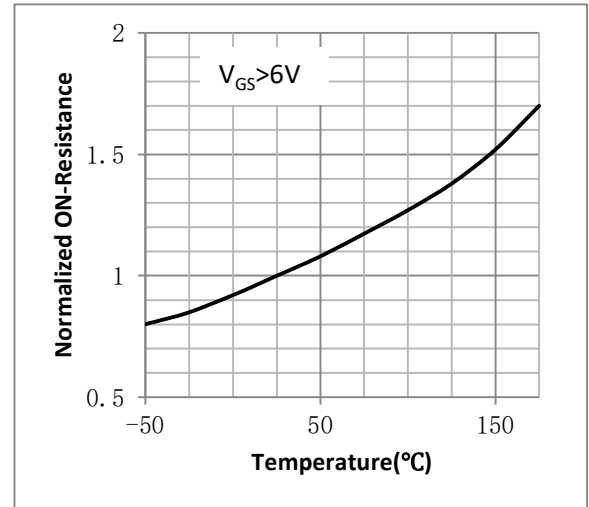


Figure 9. Diode Forward Voltage vs. Current

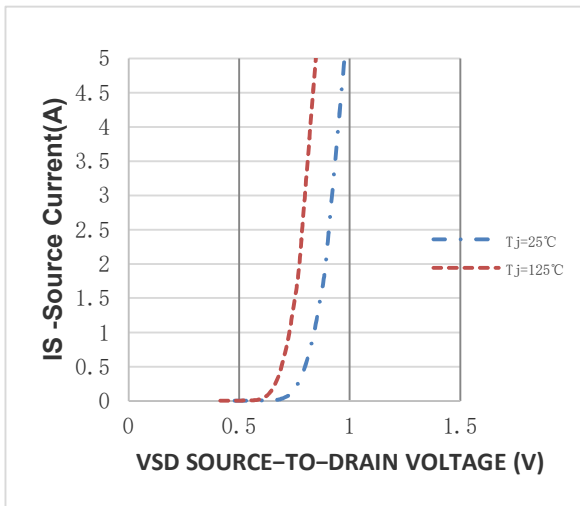


Figure 10. Transfer Characteristics

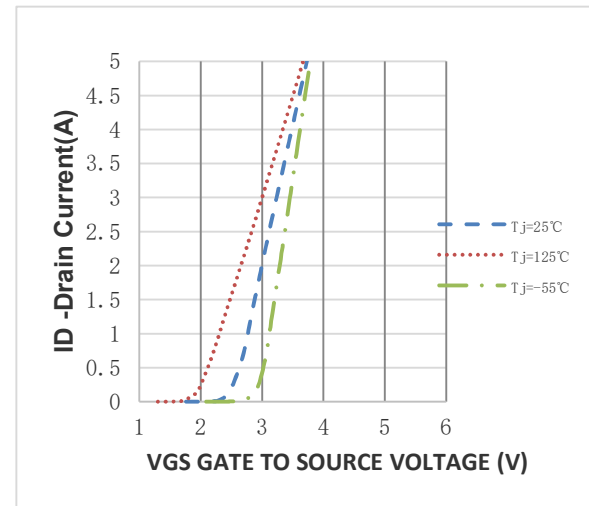


Fig.11 Safe Operating Area

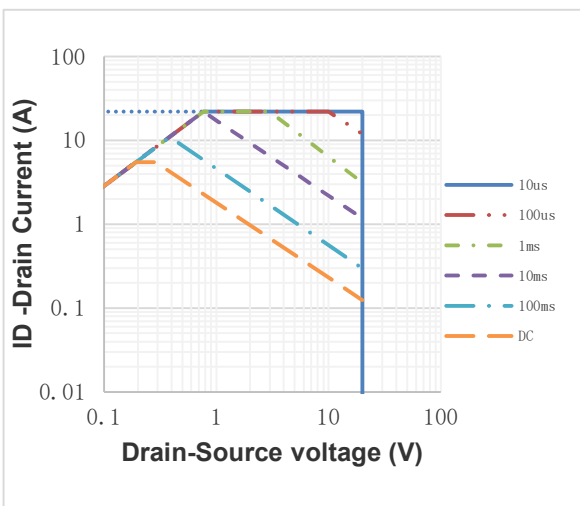
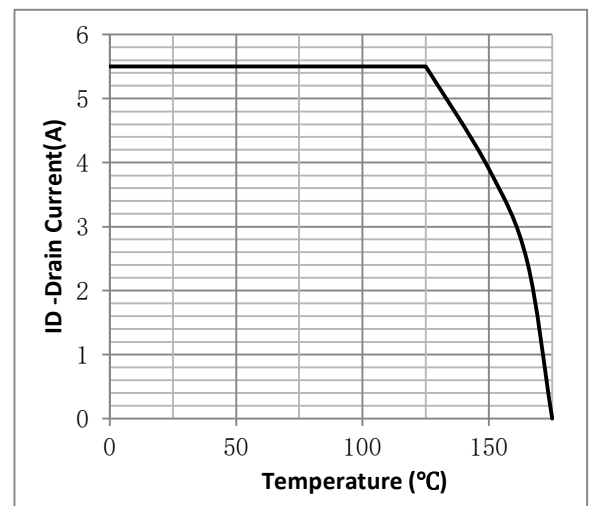


Fig.12 ID vs. Case Temperature^④



● P Channel characteristics curve

Fig.1 Gate-Charge Characteristics

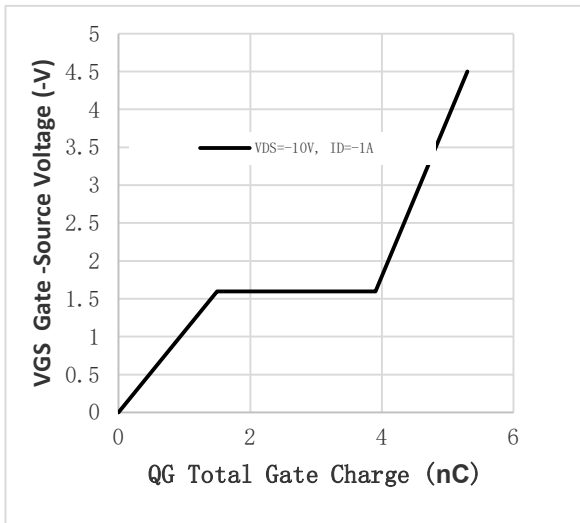


Fig.2 Capacitance Characteristics

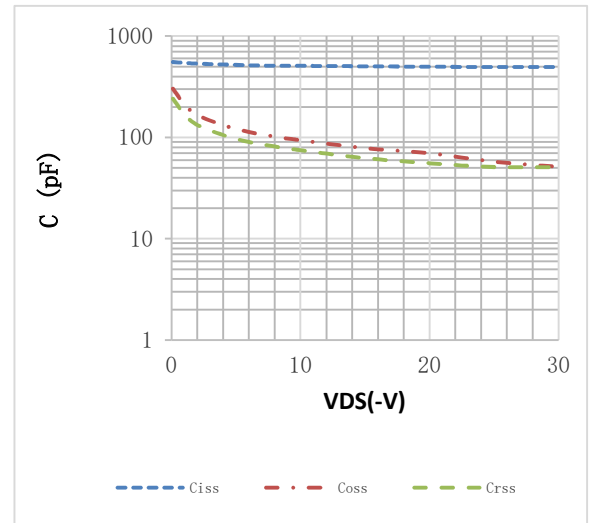


Fig.3 Power Dissipation

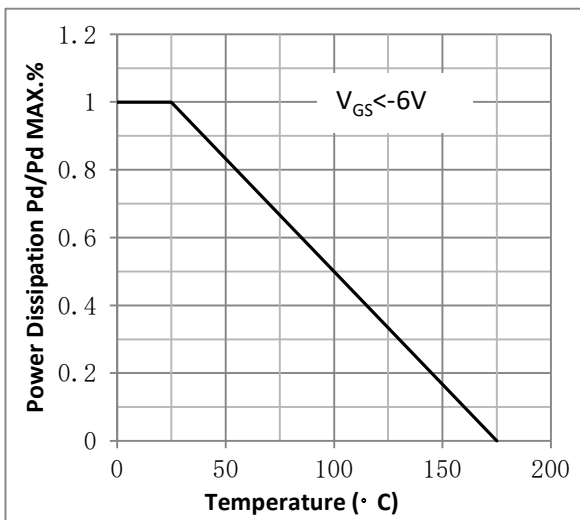


Fig.4 Typical output Characteristics

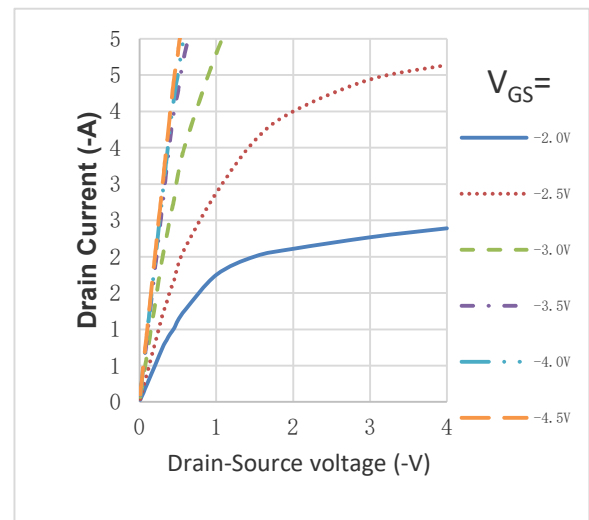


Fig.5 Threshold Voltage V.S Junction Temperature

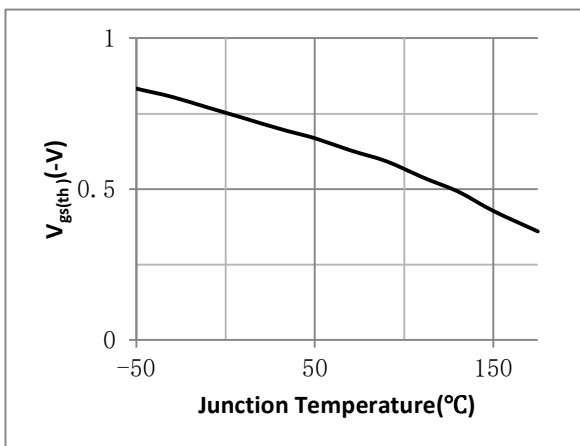


Fig.6 Resistance V.S Drain Current

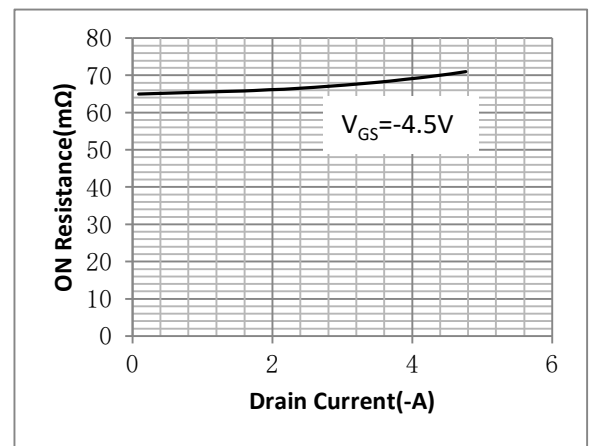


Fig.7 On-Resistance VS Gate Source Voltage

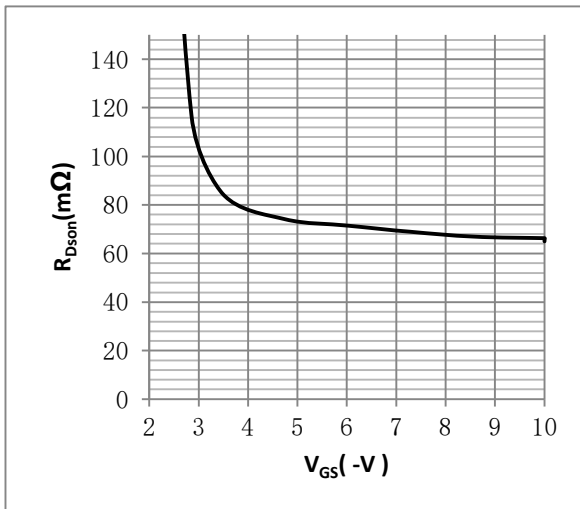


Fig.8 On-Resistance V.S Junction Temperature

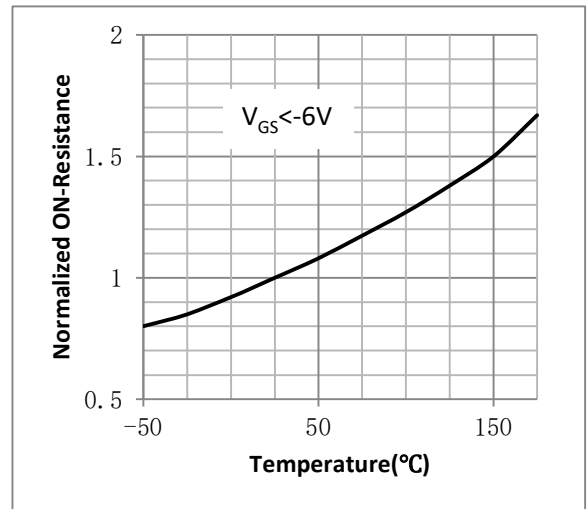


Figure 9. Diode Forward Voltage vs. Current

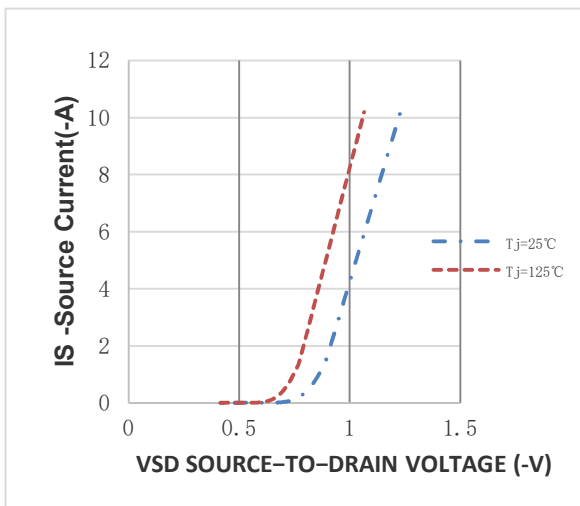


Figure 10. Transfer Characteristics

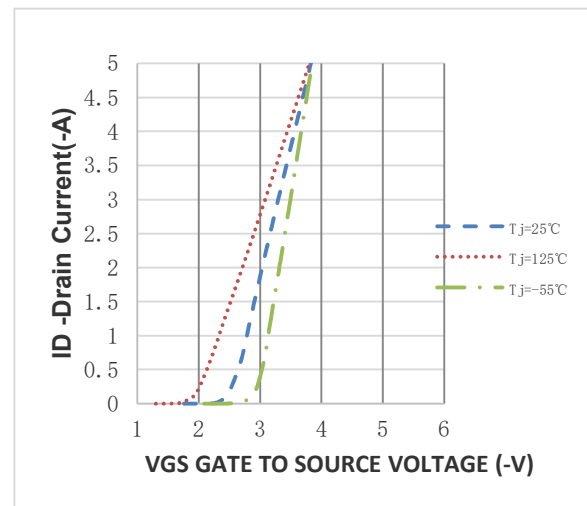


Fig.11 Safe Operating Area

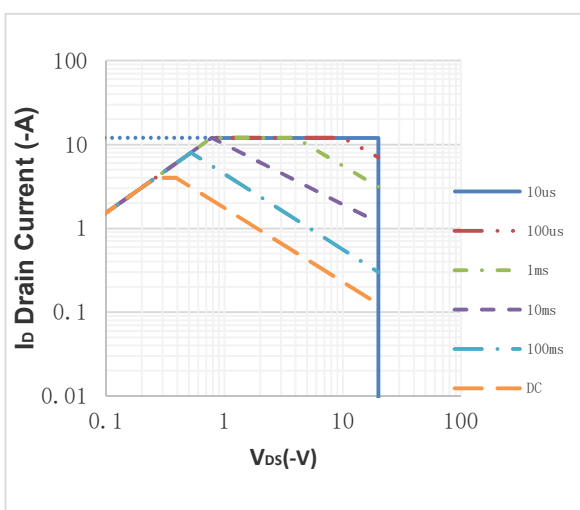
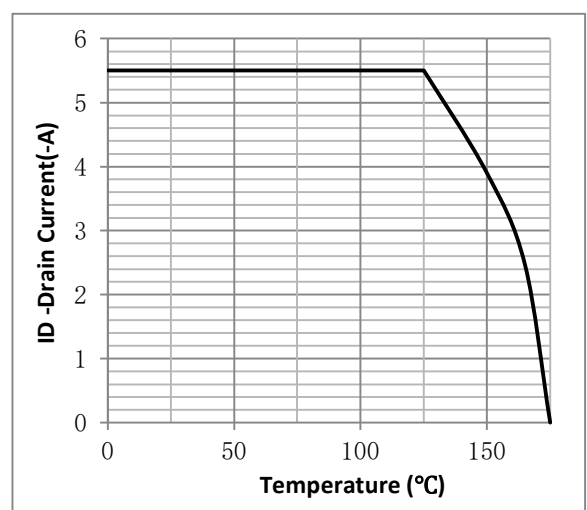
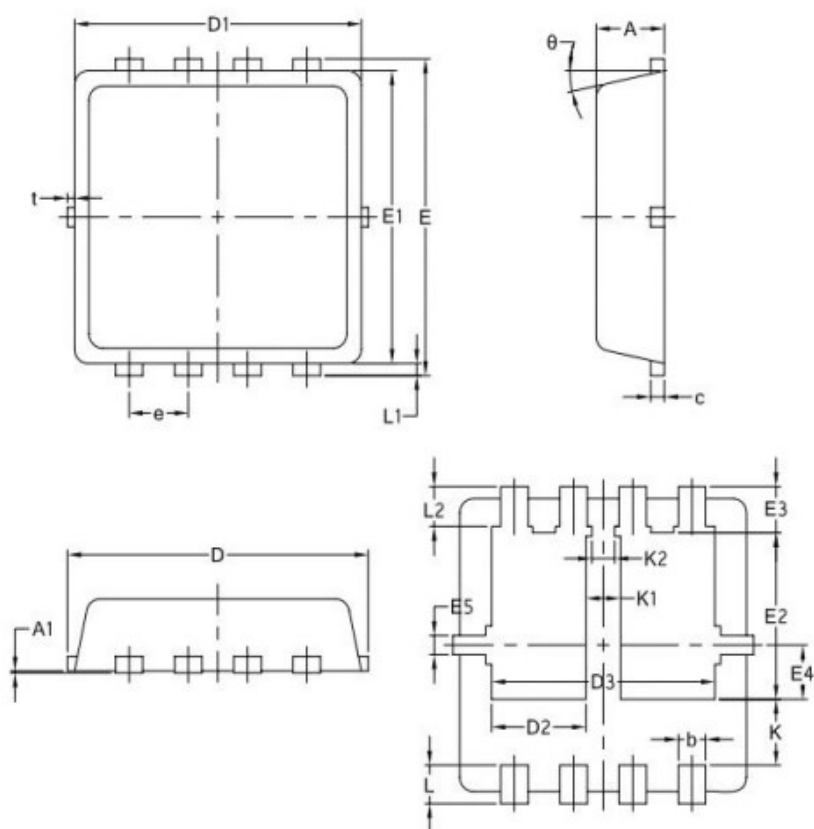


Fig.12 ID vs. Case Temperature^④



•DFN3*3 Package Outline



S Y M B O L	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
θ	10°	12°	14°

Note:

- ① Pulse : $V_{GS}=+12V/-12V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+12V/-6V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Pulse : $V_{GS}=+12V/-12V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=-12V/+6V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ③ Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ④ Practically the current will be limited by PCB, thermal design and operating temperature.
 $V_{GS}=4.5V$ (N channel)/-4.5V(P channel).

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Revision History

Version	Date	Change
A	2023.11.16	NEW
B	2025.3.21	Correct ID current.